Data Sheet | September 1998 | File Number 2896.3

600MHz, Very High Slew Rate Operational Amplifier

The Intersil HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Intersil High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/µs slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding AC parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

For further design assistance please refer to Application Note AN541 (Using the HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note AN556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers.

For military grade product information, the HA-2539/883 data sheet is available upon request.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HA1-2539-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2539-5	0 to 75	14 Ld CERDIP	F14.3
HA3-2539-5	0 to 75	14 Ld PDIP	E14.3

Features

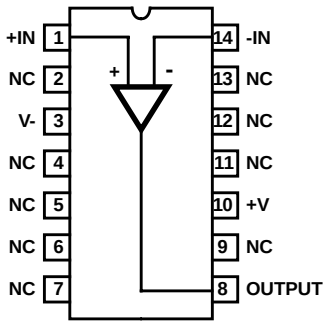
- Very High Slew Rate 600V/µs
- Open Loop Gain 15kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise . . . . . 6nV/$\sqrt{Hz}$
- Output Voltage Swing . . . . . ±10V
- Monolithic Bipolar Dielectric Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Pinout

HA-2539
(PDIP, CERDIP)
TOP VIEW



NOTE: No-Connection (NC) leads may be tied to a ground plane for better isolation and heat dissipation.

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Peak Output Current 50mA
Continuous Output Current . . . . . $33mA_{RMS}$

Operating Conditions

Temperature Range
HA-2539-2 . . . . . -55^oC to 125^oC
HA-2539-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20
PDIP Package	107	N/A

Maximum Internal Quiescent Power Dissipation (Note 1)
Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175^oC for the ceramic package and below 150^oC for the plastic package. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75^oC.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

PARAMETER	TEMP. (^oC)	HA-2539-2			HA-2539-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	25	-	8	10	-	8	15	mV
	Full	-	13	15	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	$\mu V/^oC$
Bias Current	25	-	5	20	-	5	20	μA
	Full	-	-	25	-	-	25	μA
Offset Current	25	-	1	6	-	1	6	μA
	Full	-	-	8	-	-	8	μA
Input Resistance	25	-	10	-	-	10	-	$k\Omega$
Input Capacitance	25	-	1	-	-	1	-	pF
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	V
Input Current Noise ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Voltage Noise ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	25	10	15	-	10	15	-	kV/V
	Full	5	-	-	5	-	--	kV/V
Common Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	dB
Minimum Stable Gain	25	10	-	-	10	-	-	V/V
Gain Bandwidth (Notes 5, 6)	25	-	600	-	-	600	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 3, 10)	Full	±10.0	-	-	±10.0	-	-	V
Output Current (Note 3)	25	±10	±20	-	±10	±20	-	mA
Output Resistance	25	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	25	8.7	9.5	-	8.7	9.5	-	MHz

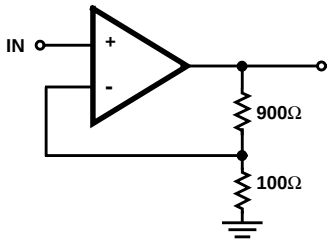
Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L < 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP. (^oC)	HA-2539-2			HA-2539-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)								
Rise Time	25	-	7	-	-	7	-	ns
Overshoot	25	-	15	-	-	15	-	%
Slew Rate	25	550	600	-	550	600	-	V/µs
Settling Time: 10V Step to 0.1%	25	-	180	-	-	180	-	ns
POWER REQUIREMENTS								
Supply Current	Full	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	dB

NOTES:

3. R_L = 1kΩ, V_O = ±10V.
4. V_{CM} = ±10.0V.
5. V_O = 90mV.
6. A_V = 10.
7. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = +5V, -15V and +15V, -5V.
10. Guaranteed range for output voltage is ±10V. Functional operation outside of this range is not guaranteed.

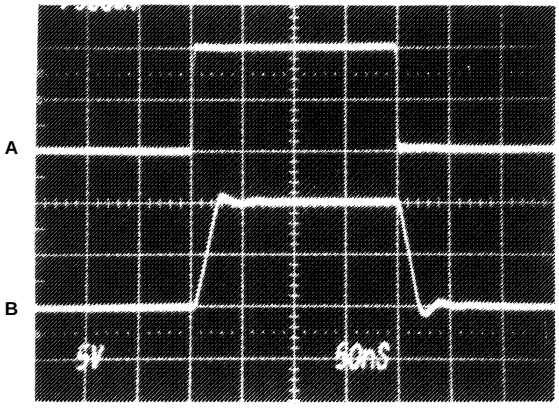
Test Circuits and Waveforms



NOTES:

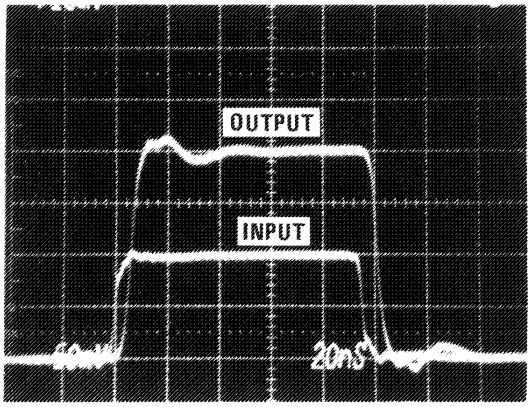
11. V_S = ±15V.
12. A_V = +10.
13. $C_L \leq$ 10pF.

FIGURE 1. TEST CIRCUIT



Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: 50ns/Div.

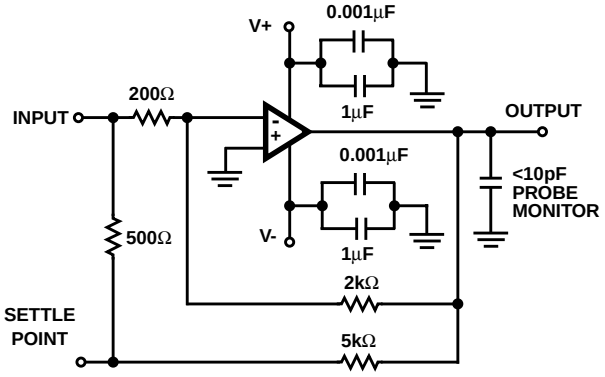
FIGURE 2. LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)

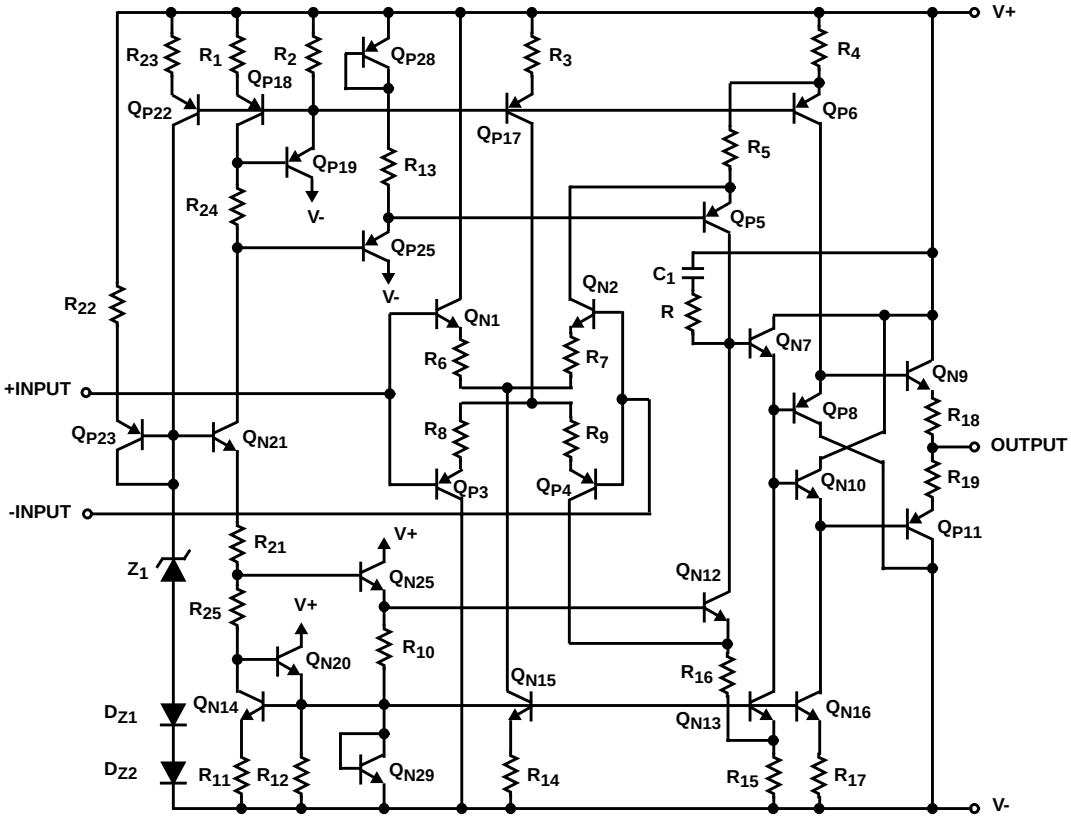


NOTES:

14. A_V = -10.
15. Load Capacitance should be less than 10pF.
16. It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
17. SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 4. SETTLING TIME CIRCUIT

Schematic Diagram



Typical Applications

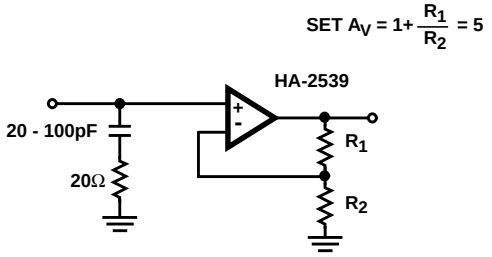


FIGURE 5. FREQUENCY COMPENSATION BY OVERDAMPING

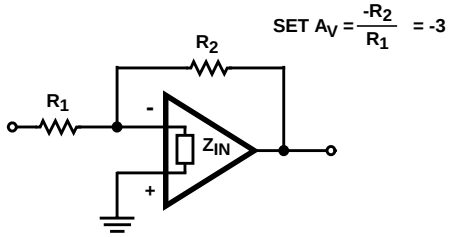


FIGURE 6. STABILIZATION USING Z_{IN}

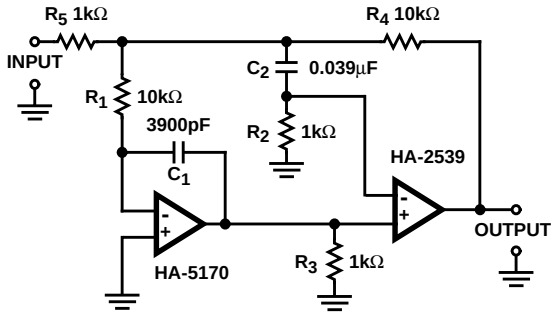


FIGURE 7. REDUCING DC ERRORS; COMPOSITE AMPLIFIER

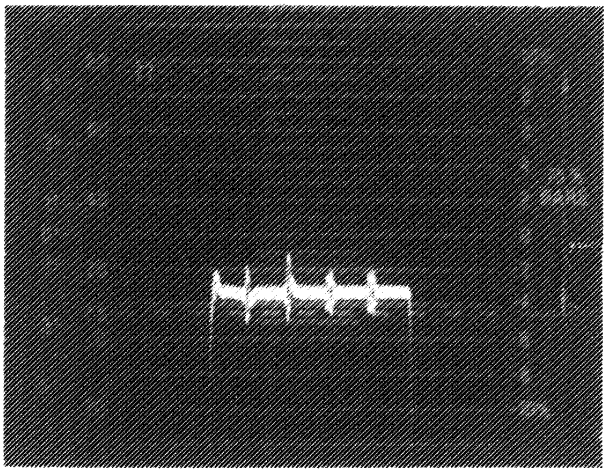


FIGURE 8. DIFFERENTIAL GAIN ERROR (3%) HA-2539 20dB VIDEO GAIN BLOCK

Typical Performance Curves

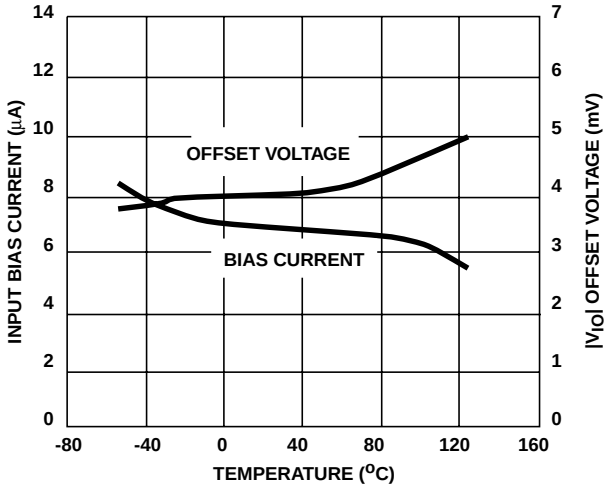


FIGURE 9. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

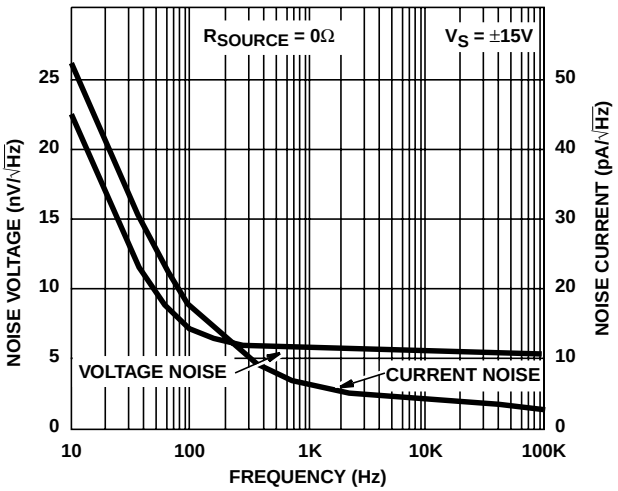


FIGURE 10. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

Typical Performance Curves (Continued)

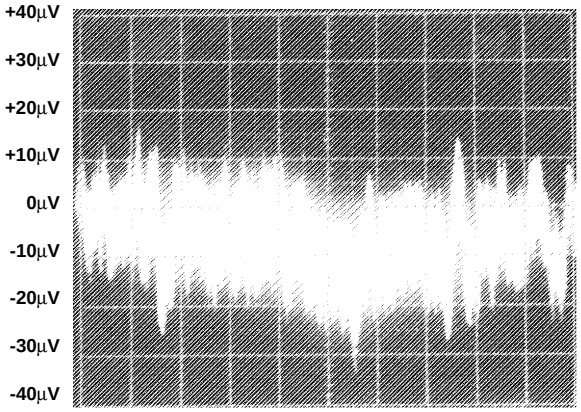


FIGURE 11. BROADBAND NOISE (0.1Hz TO 1MHz)

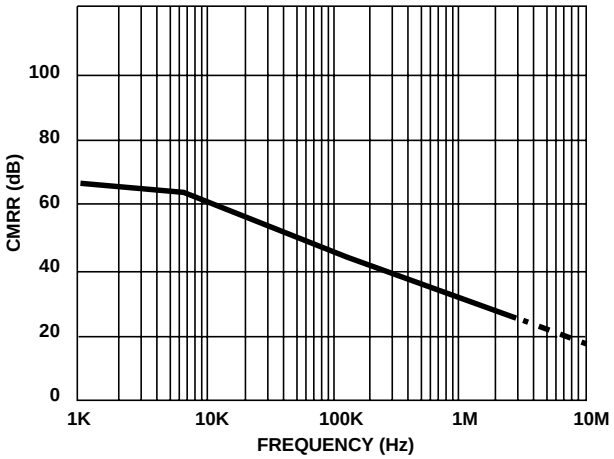


FIGURE 12. COMMON MODE REJECTION RATIO vs FREQUENCY

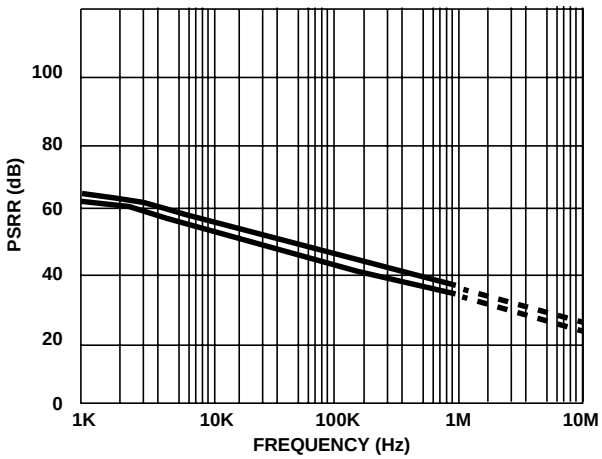


FIGURE 13. POWER SUPPLY REJECTION RATIO vs FREQUENCY

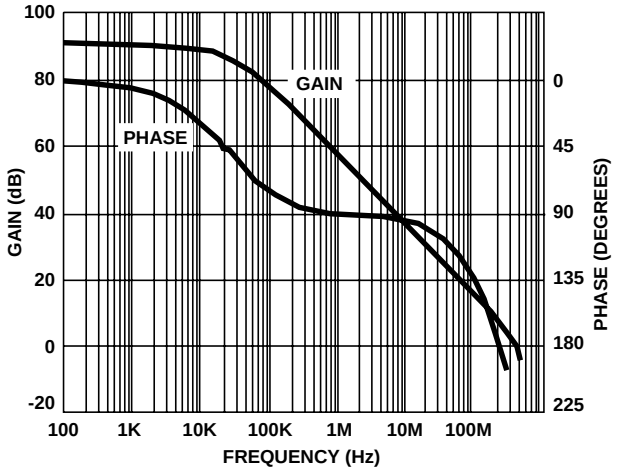


FIGURE 14. OPEN LOOP GAIN/PHASE vs FREQUENCY

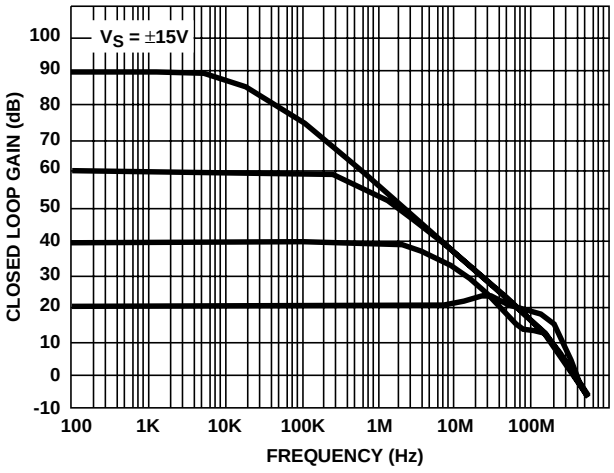


FIGURE 15. CLOSED LOOP FREQUENCY RESPONSE

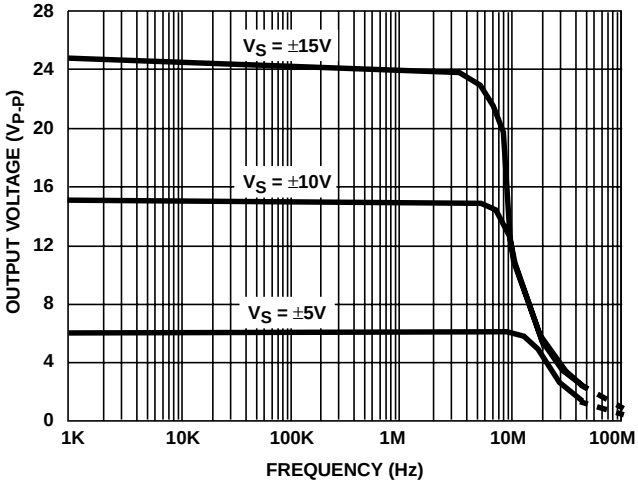


FIGURE 16. OUTPUT VOLTAGE SWING vs FREQUENCY

Typical Performance Curves (Continued)

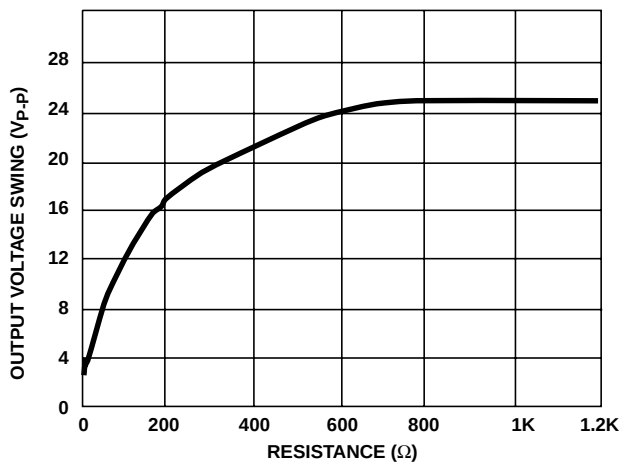


FIGURE 17. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

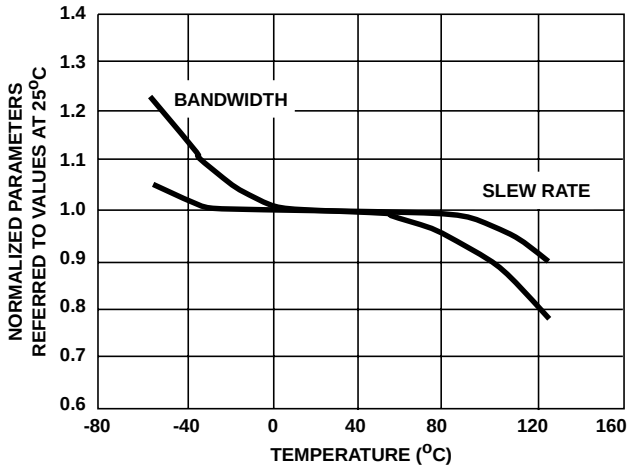


FIGURE 18. NORMALIZED AC PARAMETERS vs TEMPERATURE

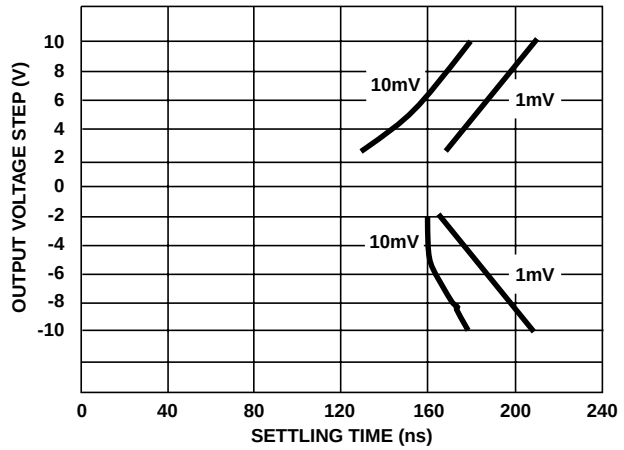


FIGURE 19. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

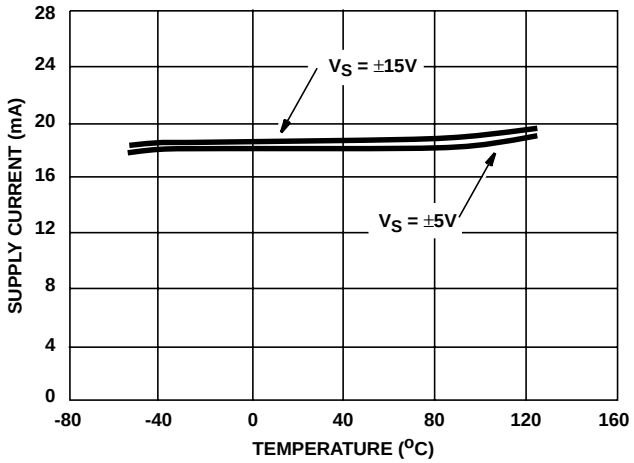


FIGURE 20. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

62 mils x 76 mils x 19 mils
1575µm x 1930µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

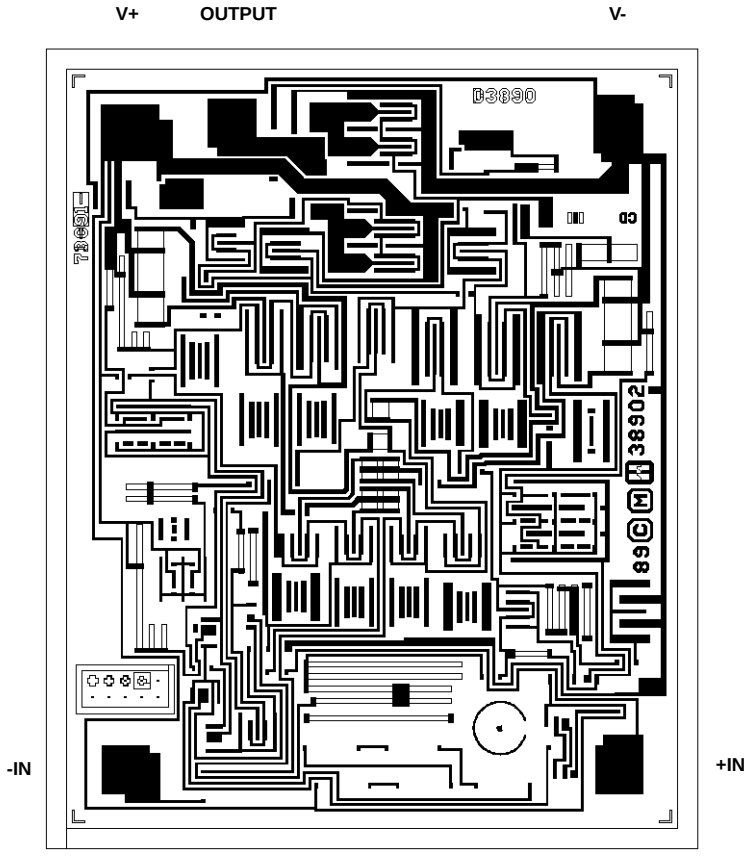
30

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2539



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